



Xilinx PLD's Systeme Developmentboards University Programm

Stefan Kouba



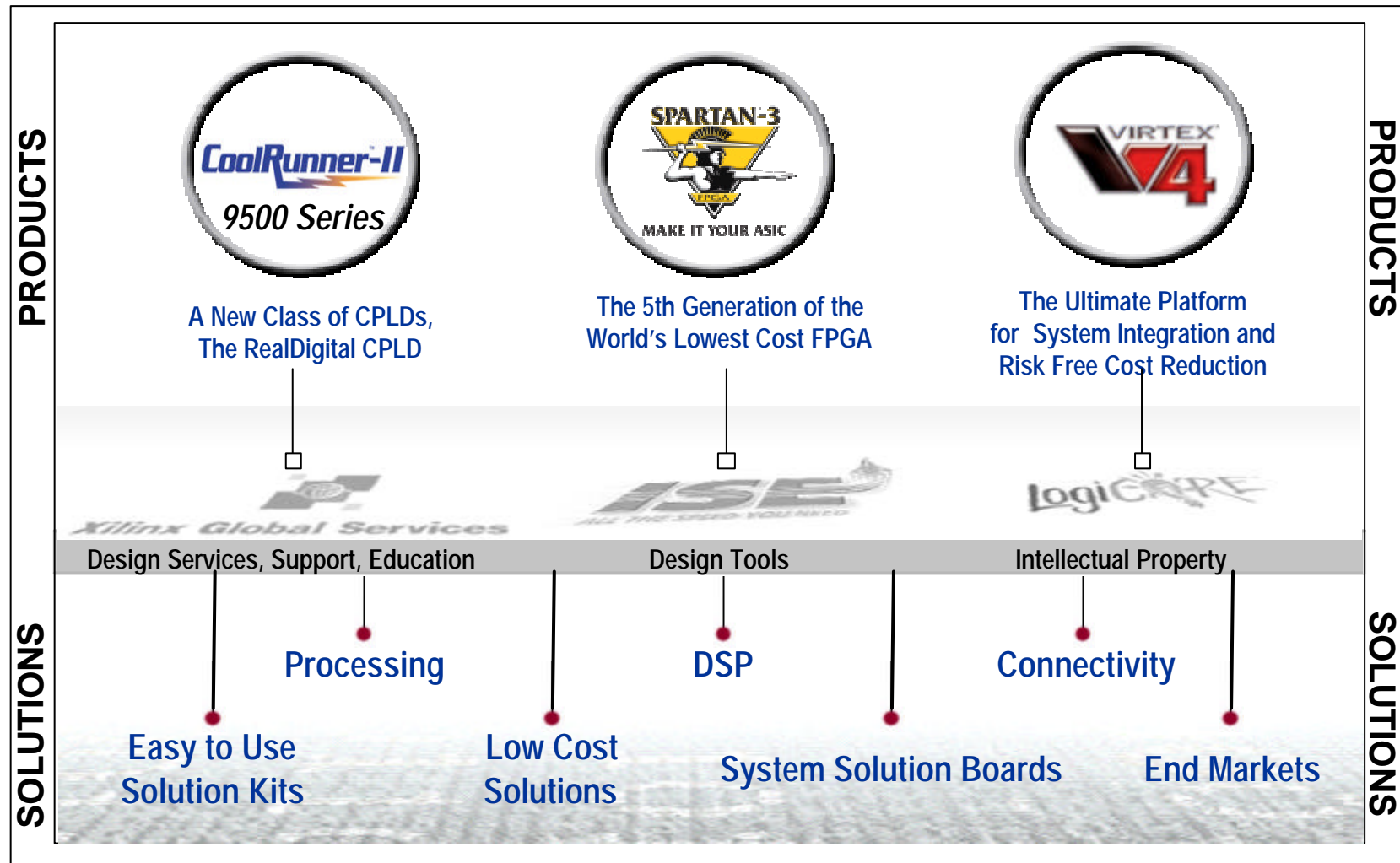
Agenda

- Xilinx – Überblick
- Produkte
 - FPGA's, CPLD's, ...
- Applikationen
 - Logik, Embedded Processor, DSP in FPGA's
- Software
 - ISE, EDK, Systemgenerator, Chipscope, ...
- Xilinx University Program
- Developmentboards





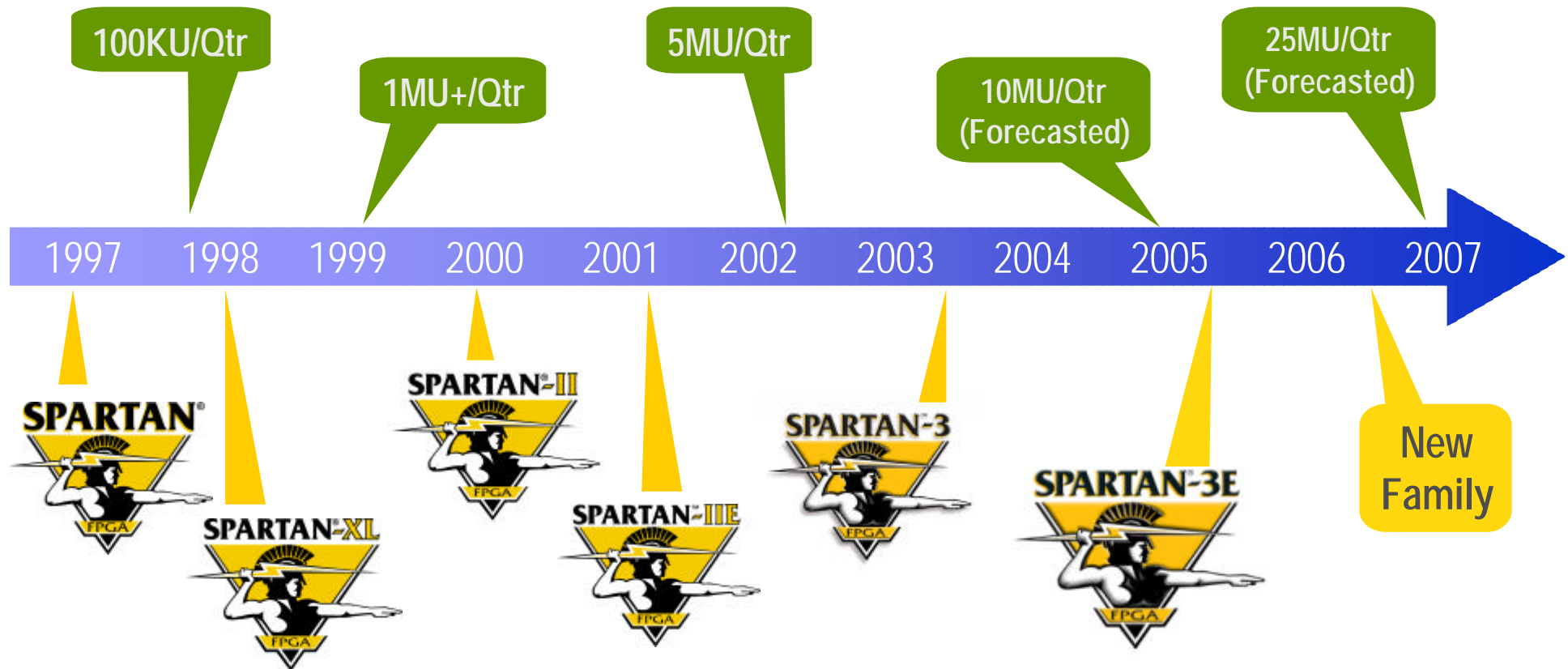
Xilinx Product Solutions



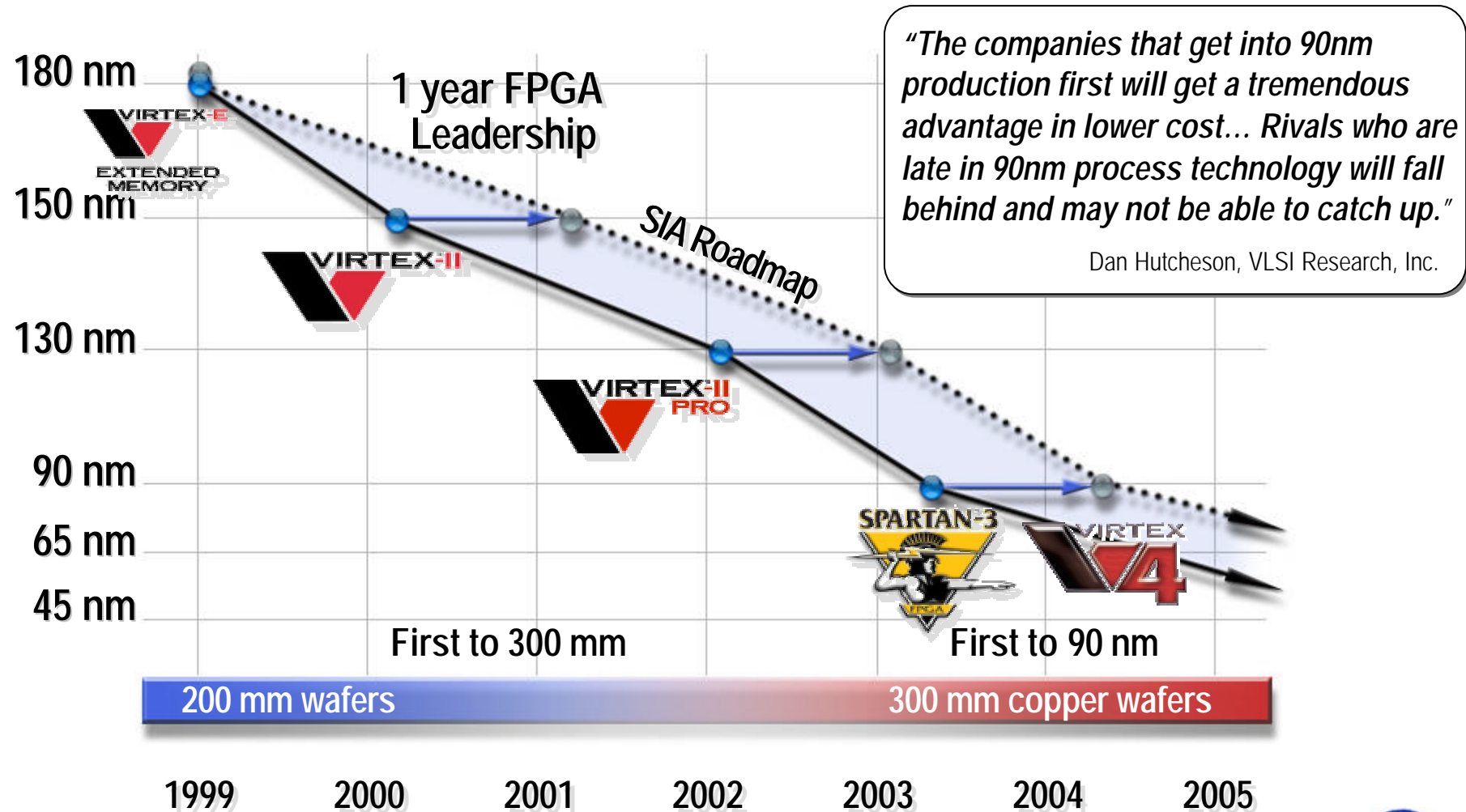


Spartan über die letzten Jahre

Key Unit Milestones



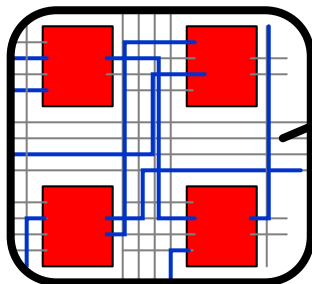
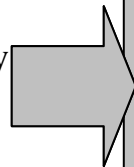
Prozess Technologien



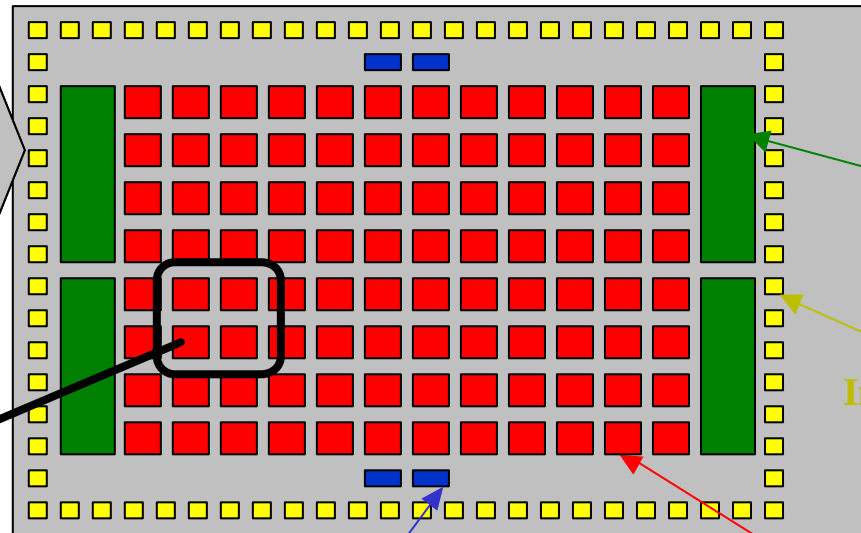


FPGA

Fully programmable.
Replace all functionality
in <50ms



Programmable Interconnect

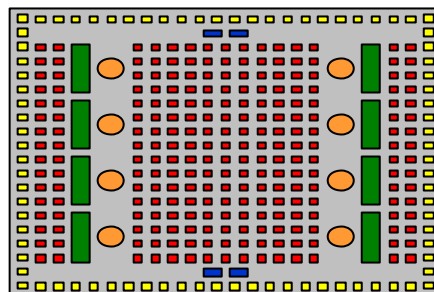


Memory Blocks

Input/Output Blocks
(IOB)

Digital Clock Management Blocks
(DLL or DCM)

Configurable Logic blocks
(CLB)



XC3S50

192 CLB



4 RAM



4 Multipliers

XC3S5000

8320 CLB



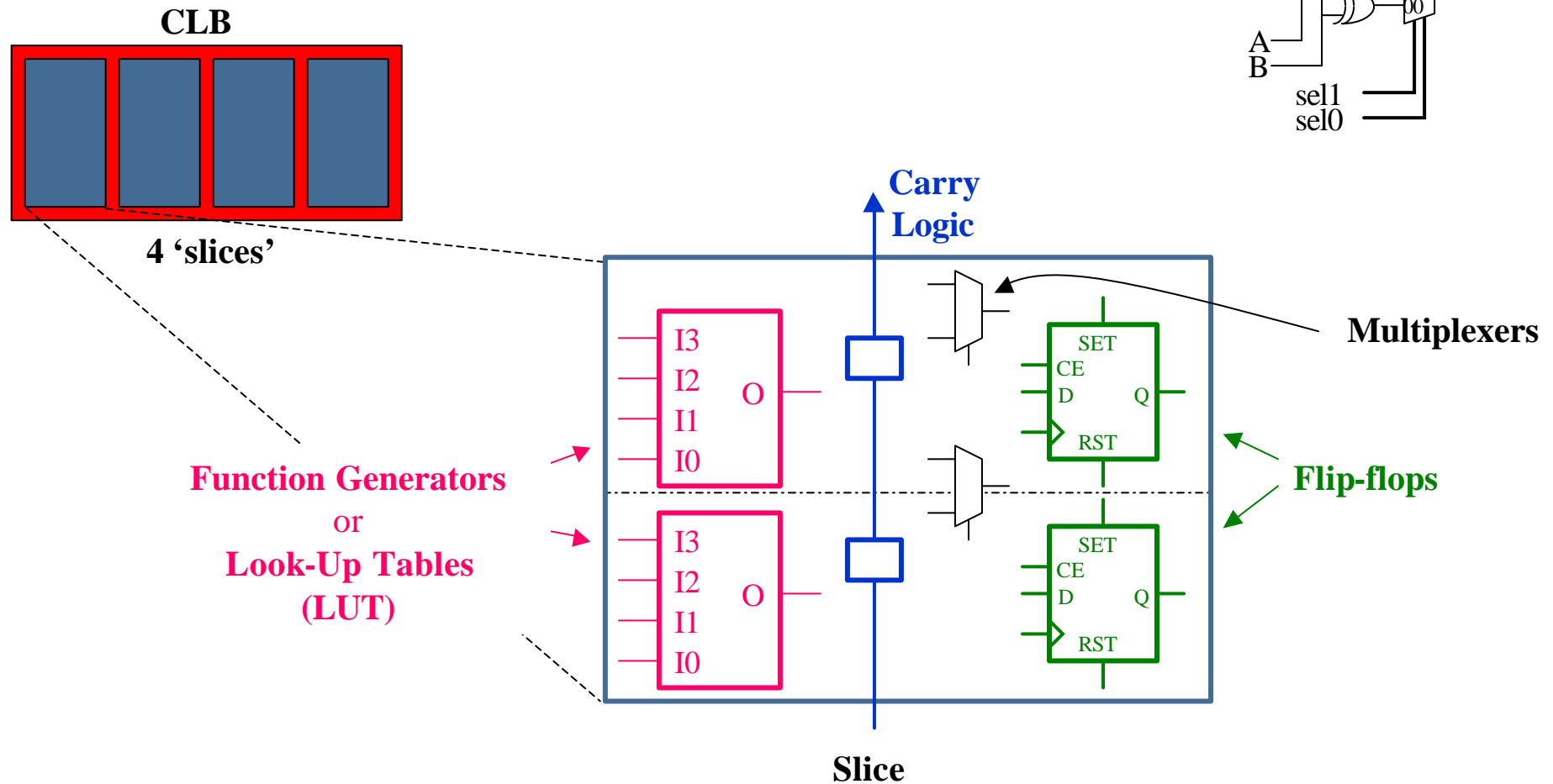
104 RAM



104 Multipliers



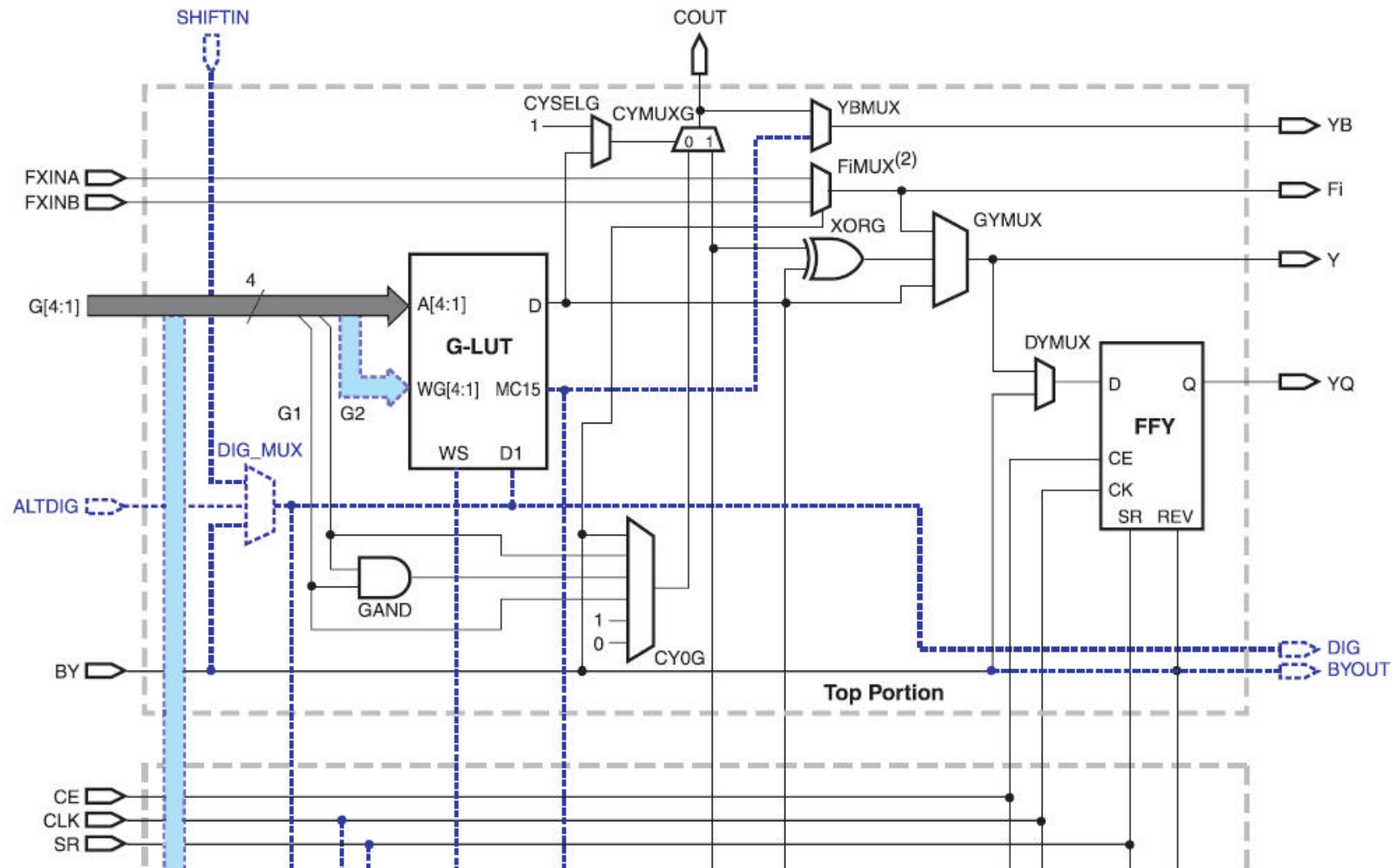
CLB's und Slices



2 FlipFlops, 2 Look Up Tables, Carry Logic



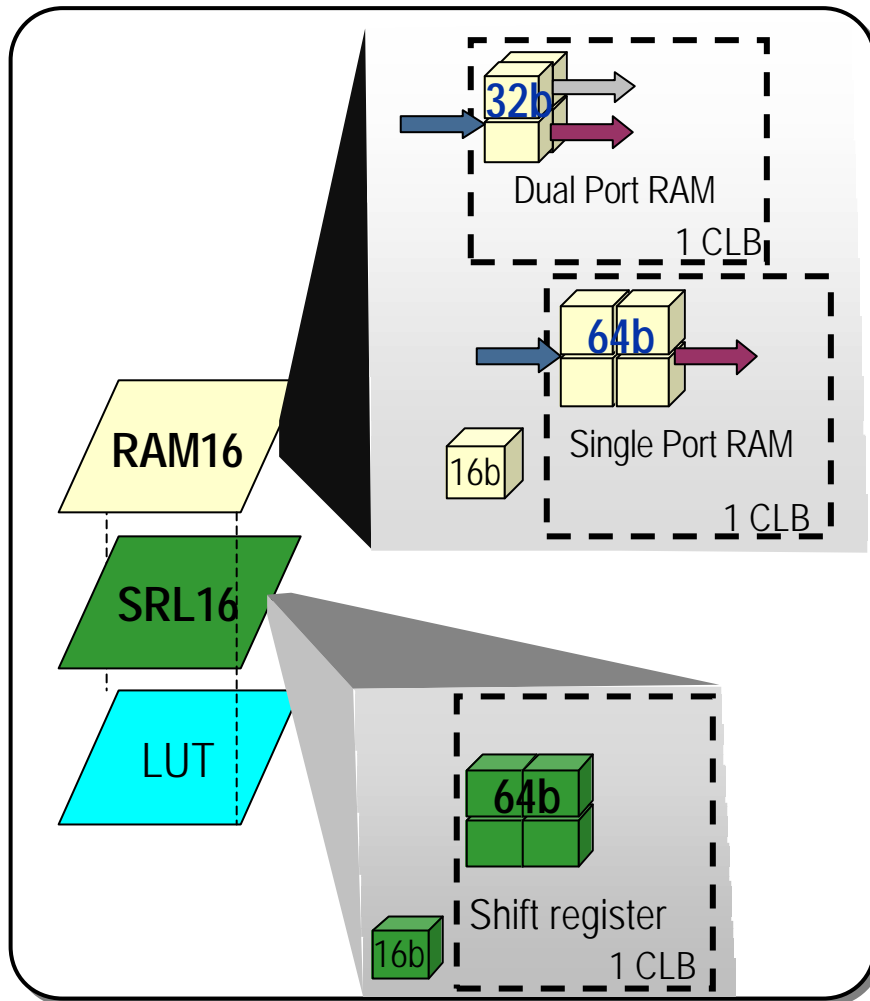
Screenshot Slice





Distributed RAM

Flexible LUT Struktur

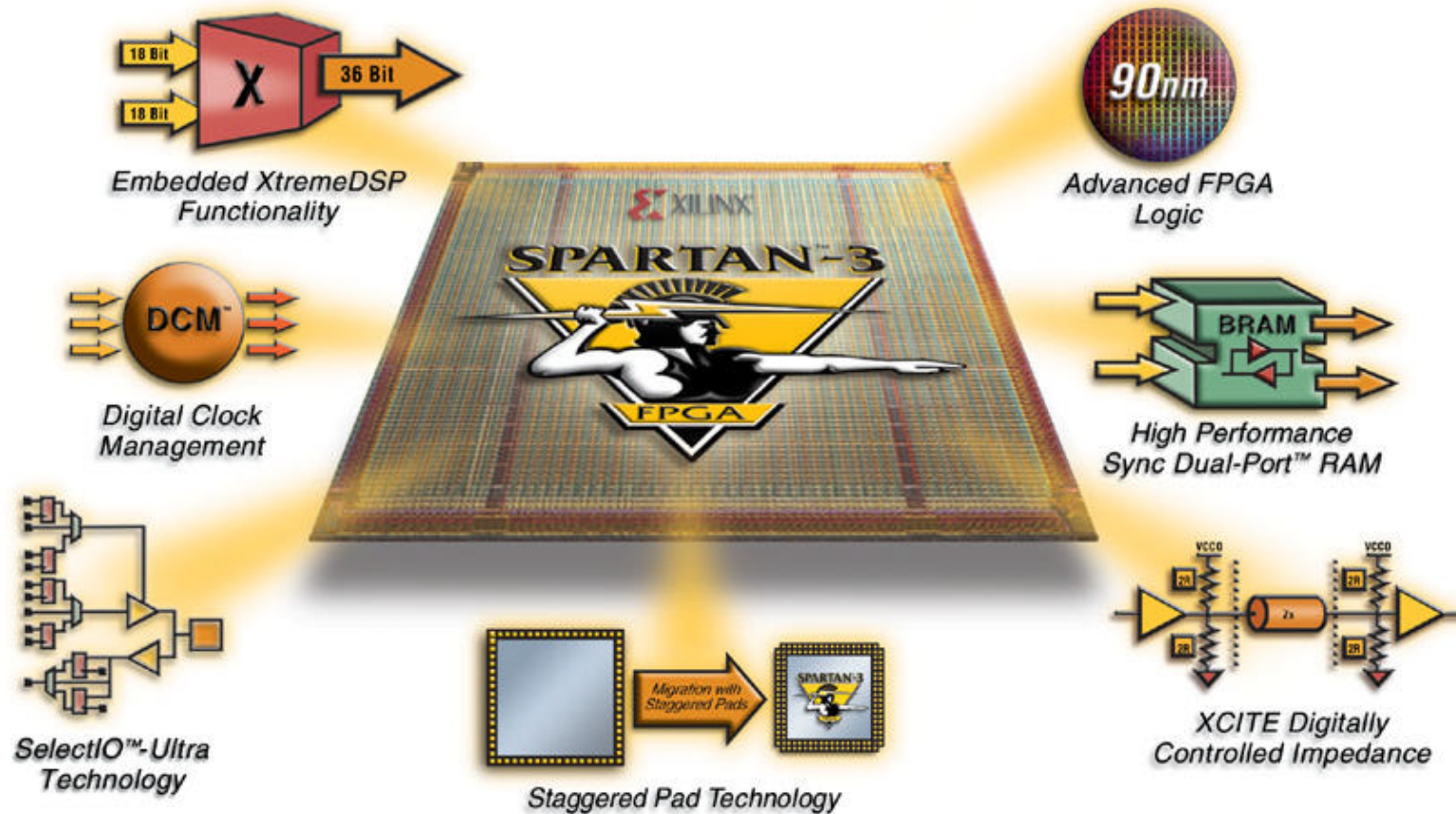


- Kann als Logik, RAM, ROM, oder Schieberegister instantiiert werden
 - 1 CLB = 32bit Dual Port RAM
configurations: 16x1
 - 1 CLB = 64bit Single Port RAM
configurations: 16x1, 32x1, 48x1 and 64x1
 - 1 CLB = 64bit Shift Register
- Kaskadierbar CLB Routingressourcen
- Schnelle Zugriffszeiten
- Anwendungen
 - Linear Feedback Shift Register, Schedule multiplies, Small FIFO, Digital delay lines



Spartan-3

A New Class of Spartan FPGAs

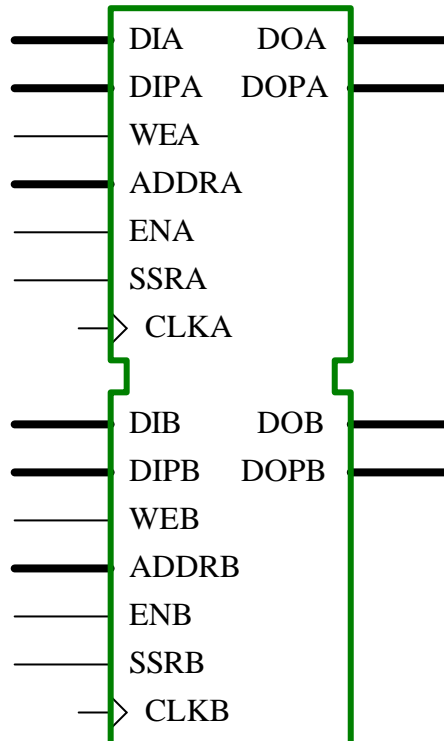




Spartan-3 Block RAM



18-kbits



- Dual Port Block RAM
- Voll synchroner Zugriff (Schreibe/Lese)
- Variable Bitbreitendefinition

Data Width	Parity Bits	Memory locations	Address Width
1	-	16384	14
2	-	8192	13
4	-	4096	12
8	1	2048	11
16	2	1024	10
32	4	512	9

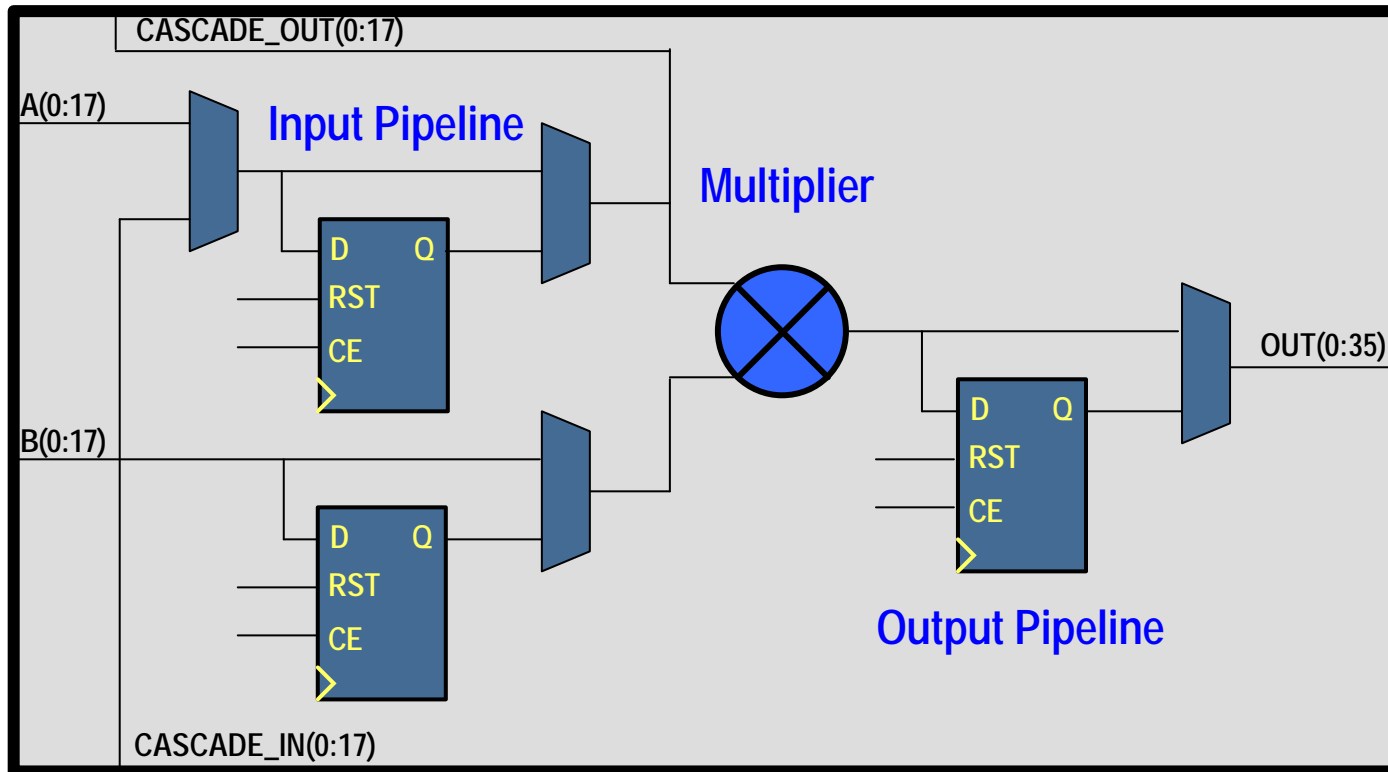
DOA = 9 x 1024

DOB = 16 x 512





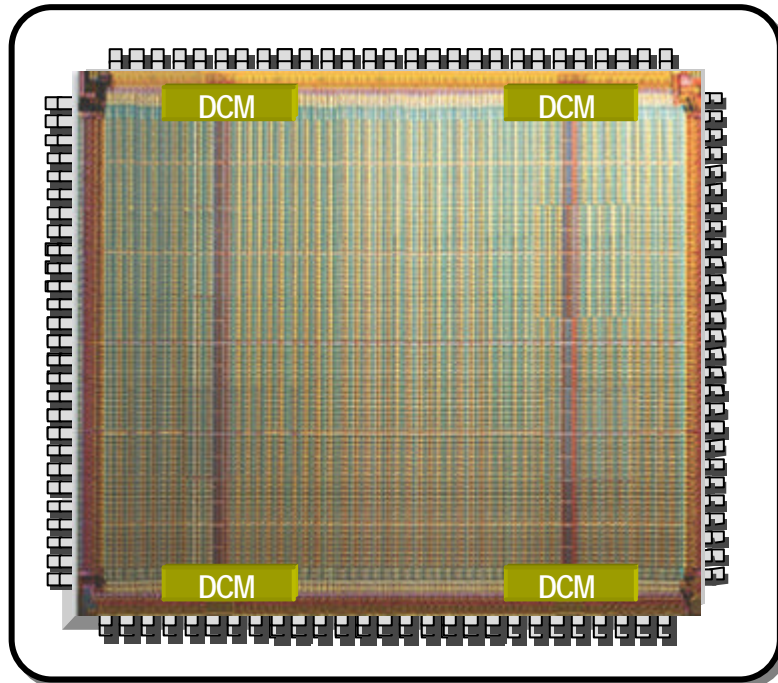
Spartan-3E Multiplizierer



- Pipeline -> DSP Applikationen
- Kaskadierbar für weitere Bitbreiten



Digital Clock Manager (DCM)



- 4 DCMs; located at top and bottom of the Block RAM columns

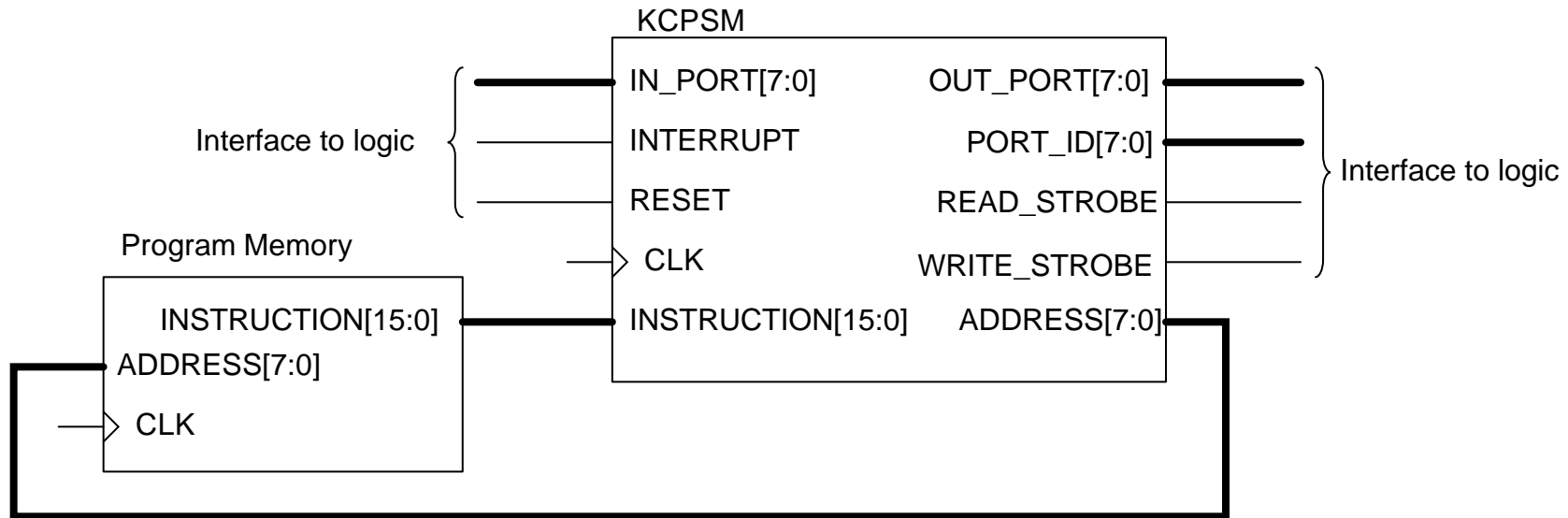
- Clock phase de-skew
- 50% duty cycle correction
- DLL performance
 - 5 MHz to 326 MHz
 - 100 ps Jitter
- Phase Shift (PS)
 - 0, 90, 180, 270
 - CLK Period/256
- Digital Frequency Synthesis (DFS)
 - m/n clock multiply & divide
 - $m = 2$ to 32, $n = 1$ to 32
- Temperature compensation



PicoBlazeTM

8-bit micro controller – frei zur Verfügung stehende VHDL Source Code unter:

http://www.xilinx.com/ipcenter/processor_central/picoblaze/index.htm



Programm Memory:

Single Block RAM configured as a 256×16 ROM
100% Embedded Solution

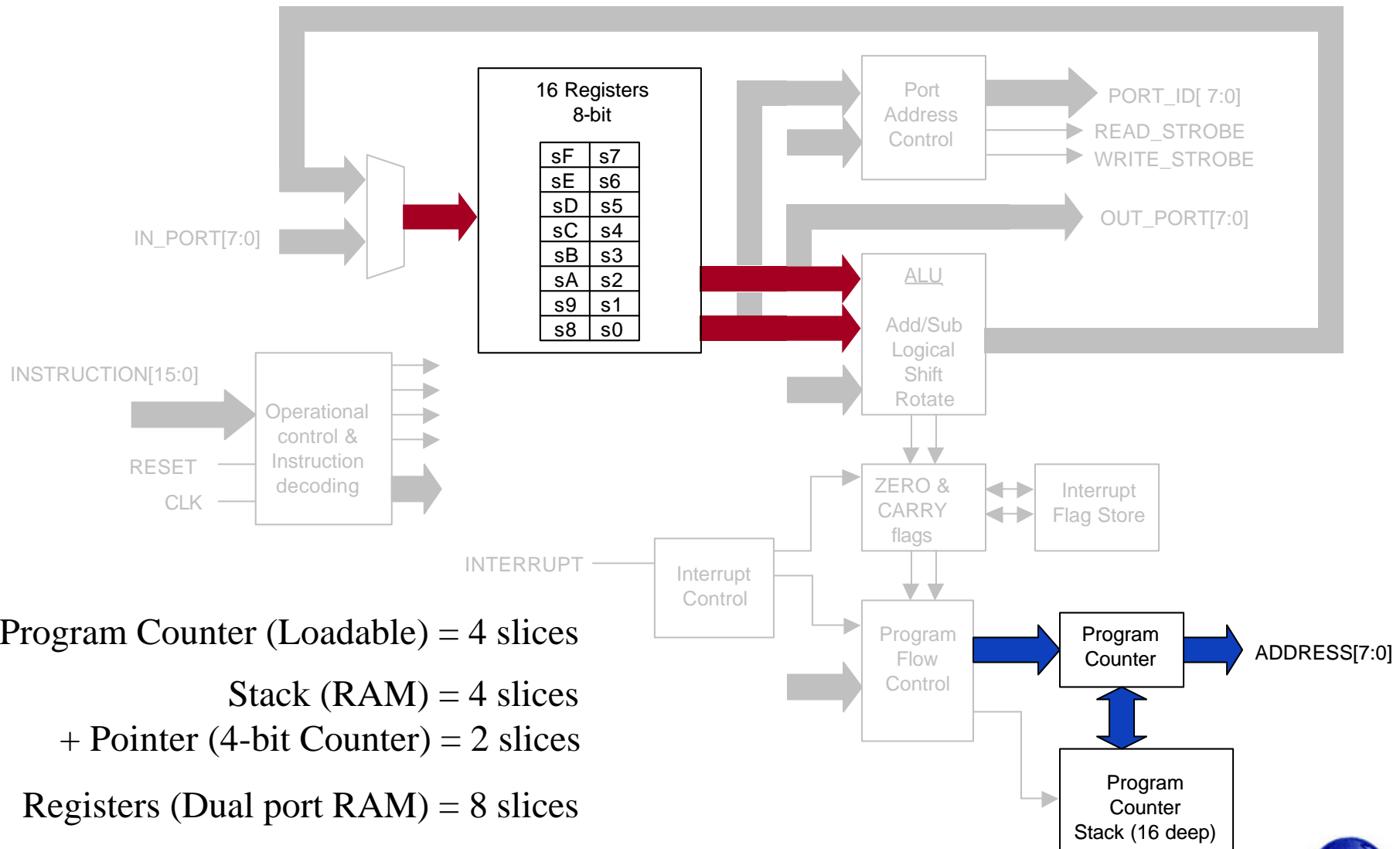
Features

8-bit Data
16 Registers
Interrupt
Reset

Built-In CALL & RETURN Stack



PicoBlaze



Program Counter (Loadable) = 4 slices

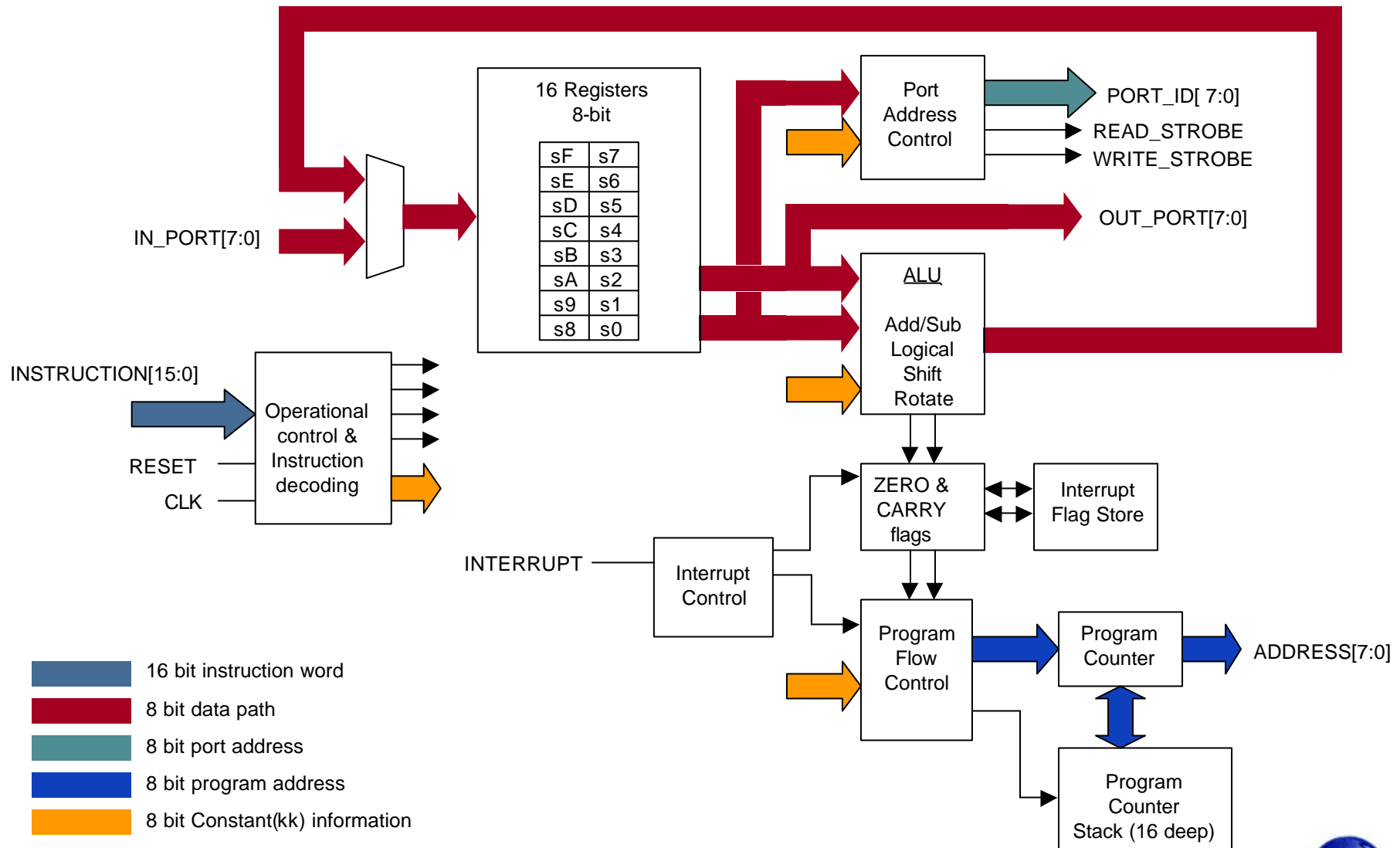
Stack (RAM) = 4 slices
+ Pointer (4-bit Counter) = 2 slices

Registers (Dual port RAM) = 8 slices

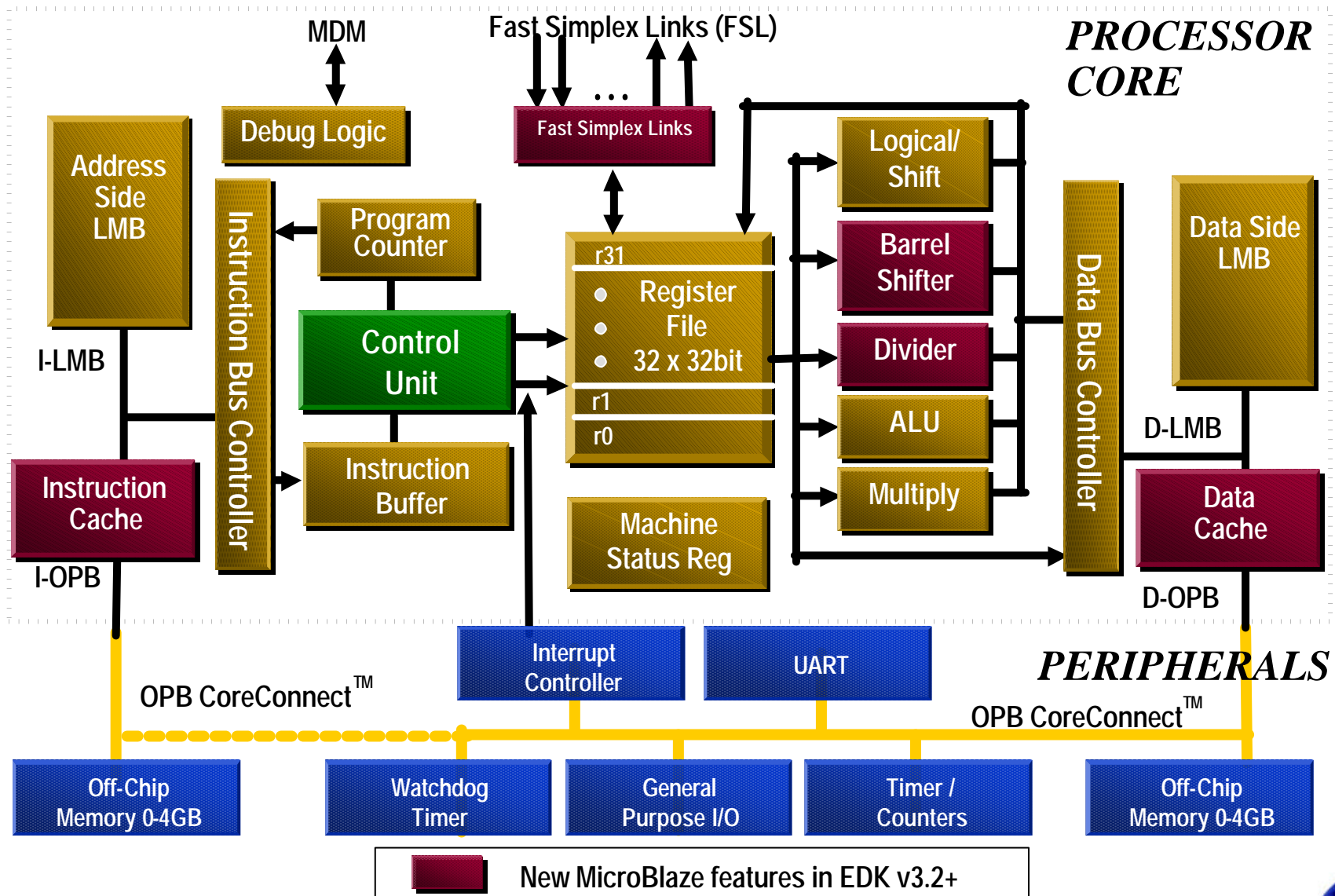


PicoBlaze

Here is the architecture of PicoBlaze. The instruction set is on the next page.....



MicroBlaze System Diagram





Virtex-4



200,000
Logic Cells



500 MHz
Differential Clocking



500 MHz BRAM



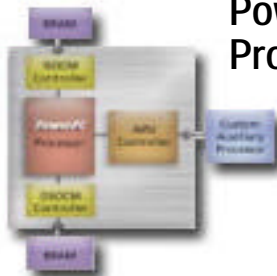
0.6-11.1 Gbps
RocketIO™
Transceivers



AES Secure Chip
Design Security



1 Gbps SelectIO™
with ChipSync™

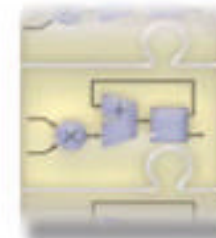


PowerPC®
Processor with APU



10/100/1000
Ethernet MAC

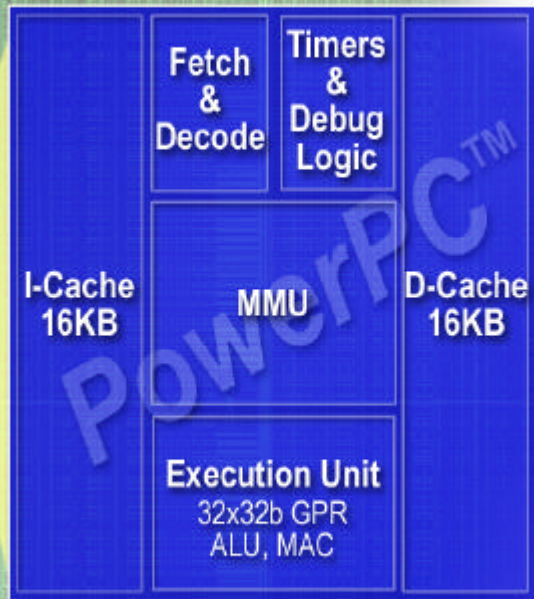
500 MHz
XtremeDSP™ Slice





Integrierter PowerPC 405

Beliebteste Embedded Processor Architektur

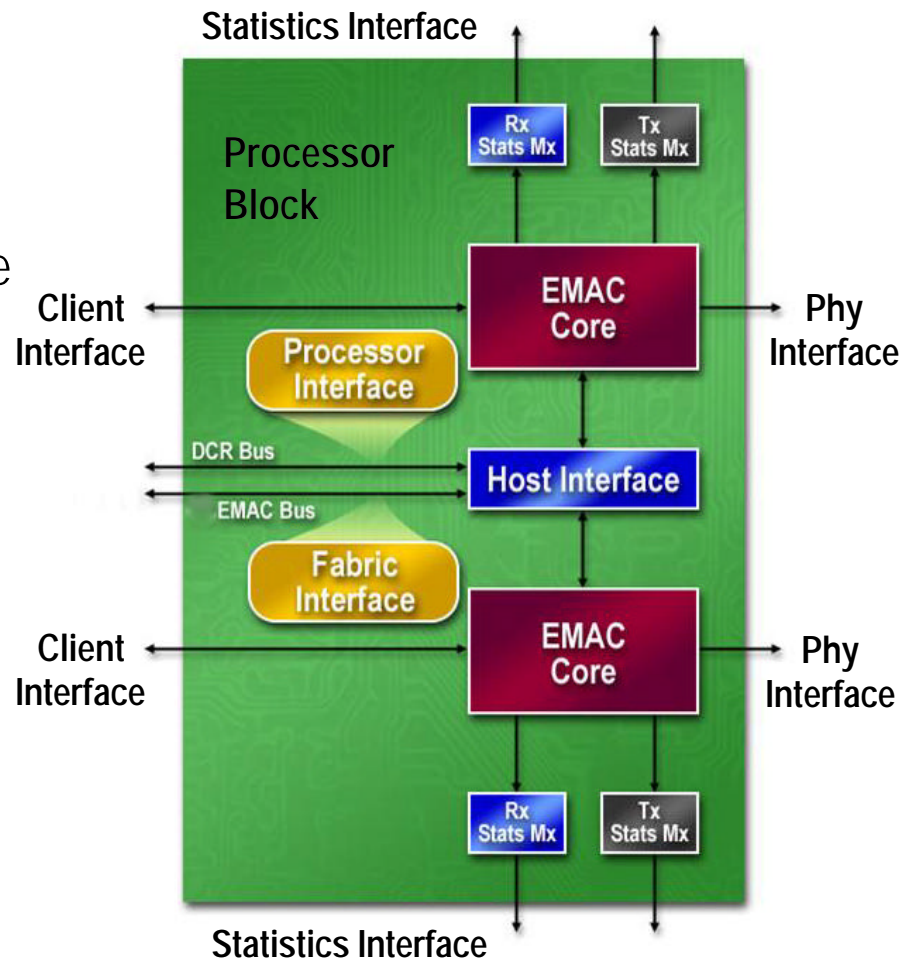


- **High-performance**
 - 680 DMIPS@ 450MHz
- **Low power**
 - 0.29mW/MHz
- **zweite FPGA Generation mit PPC 405**
 - HW und SW IP
 - CoreConnect™ Bus Architektur
 - System-level IP
- **Neues APU interface**
 - Direktzugriff vom FPGA fabric auf PowerPC core
 - Microcontroller und Co-Prozessor support



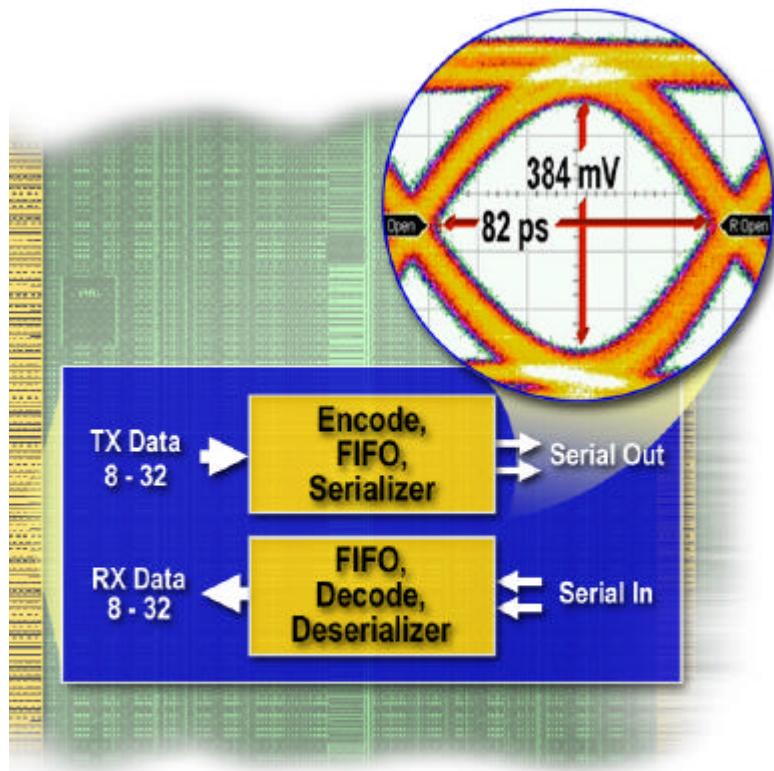
New Tri-Mode Ethernet MAC

- Voll integrierter Ethernet Media Access Controller (EMAC)
 - 10/100/1000 Mbps
 - 2 oder 4 cores pro Virtex-4 FX Device
- UNH-Compliant
- Mit PowerPC oder stand-alone
- Key benefits
 - Erspart 4000 Logiczellen pro Ethernet MAC
 - Implementiert single-chip 1000 Base-X Ethernet
 - Network management oder FPGA monitoring





Rocket IO's

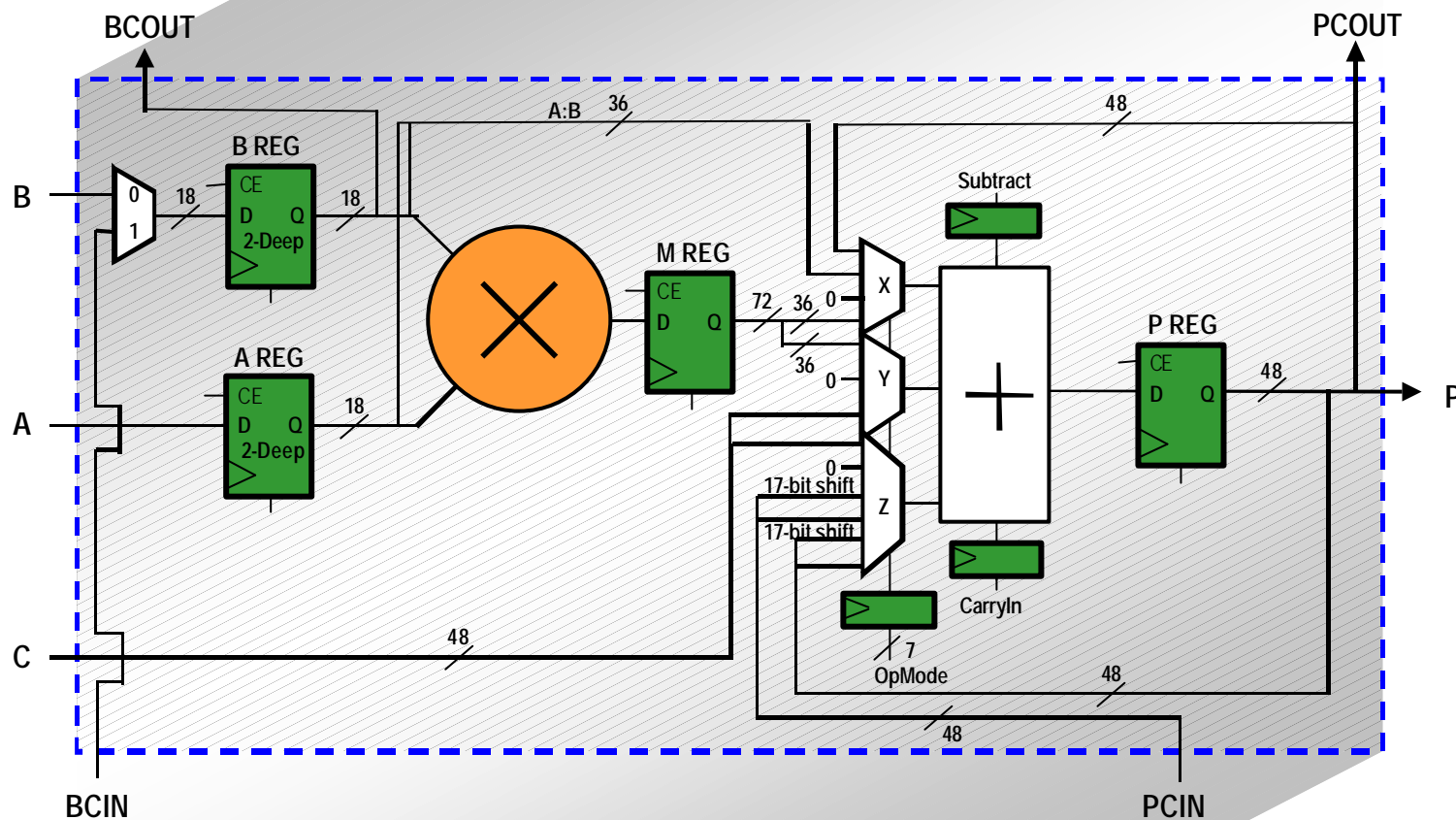


- Virtex-4 RocketIO™ Transceivers
 - Full-duplex serielle Transceiver Blöcke mit integrierter SERDES und Clock/Data Recovery (CDR)
- 622 Mbps - 11.1 Gbps
- Kompatibel mit Virtex-II Pro
- Chip-to-chip, Backplane, Chip-to-Optics





The XtremeDSP Slice



500 MHz maximum frequency in the fastest speed grade



Xilinx ISE Design Tool



- FREE Web download or CD
- Virtex-4 LX15, LX25
- Up to Spartan-3 1500
- All CPLDs



- Core Generator and FPGA Editor
- \$695 list price
- Virtex-4 LX15, LX25, SX25, FX12
- Up to Spartan-3 1500
- All CPLDs



- Linux-64 and Solaris support
- ISE Simulator Lite
- Core Generator and FPGA Editor
- \$2495 list price
- All Virtex-4 FPGAs
- All Spartan-3 Series FPGAs
- All CPLDs



\$695

FPGA real-time debug

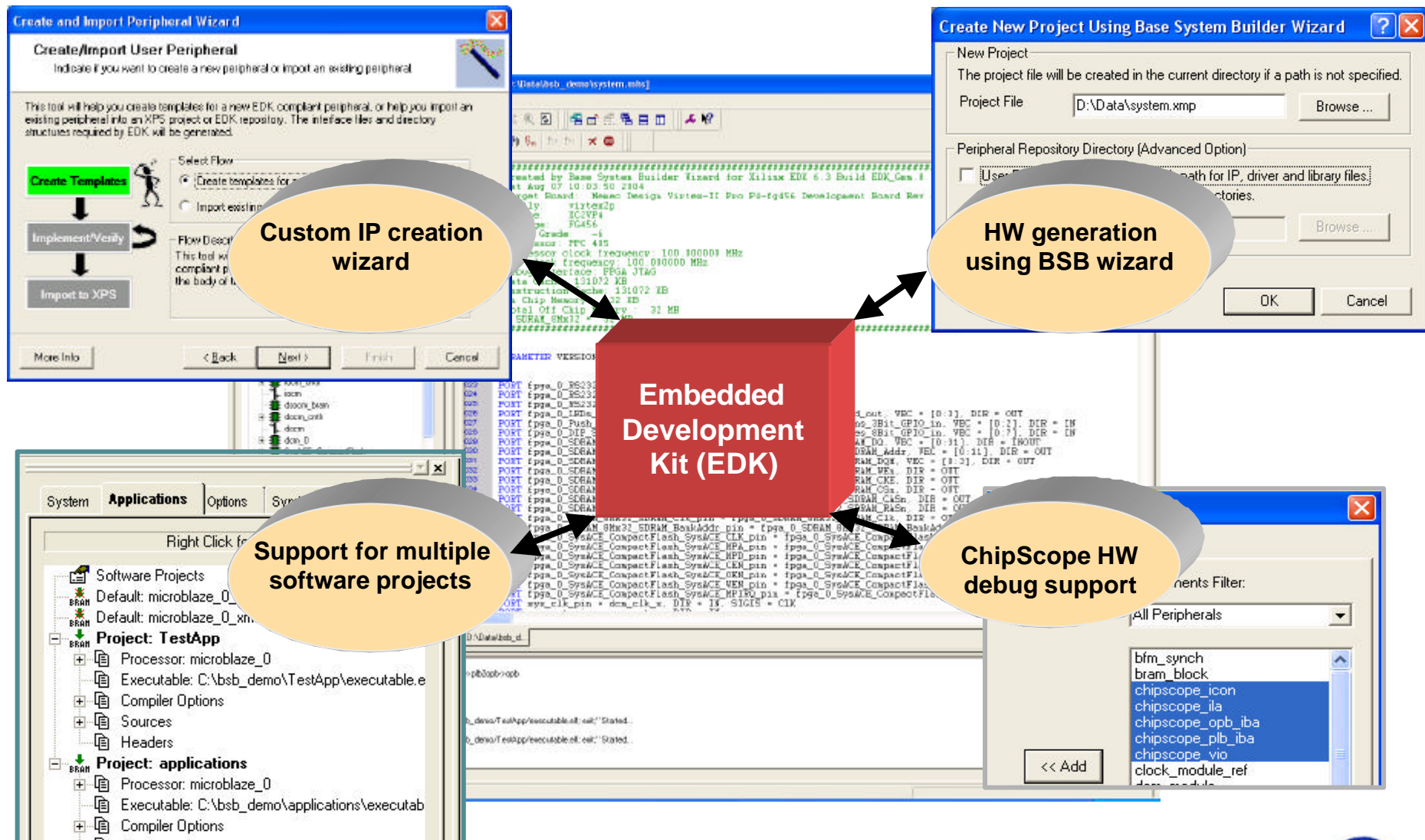


\$945

HDL simulator

Evaluation Versionen verfügbar

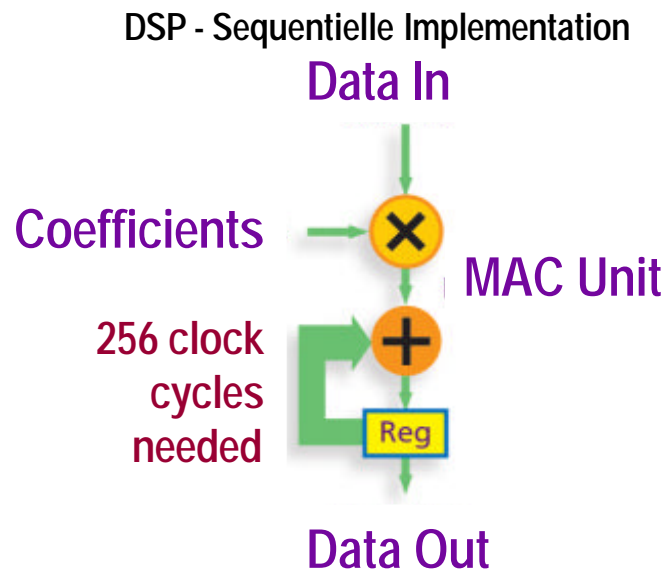
Embedded Development Kit



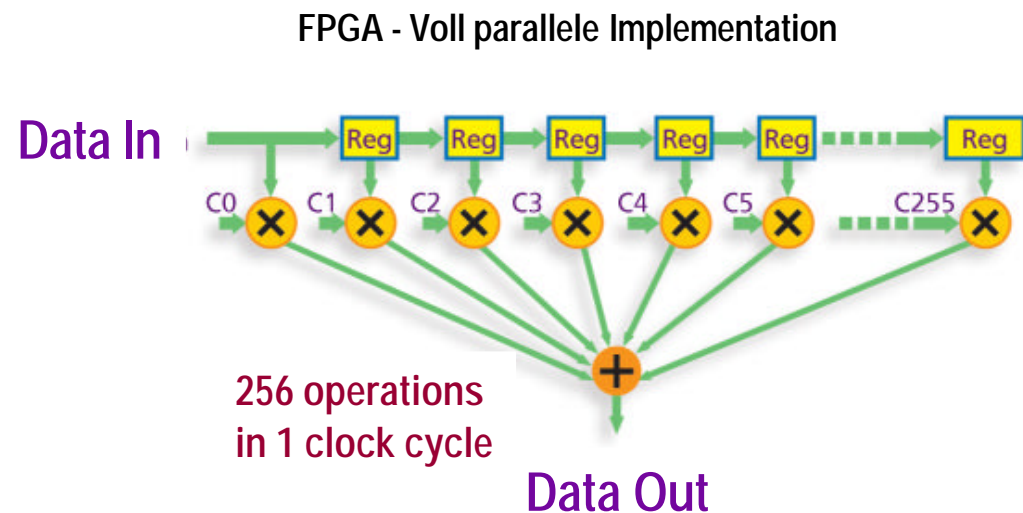


Warum FPGA's für DSP's

z.B. 256 Tap FIR Filter Implementation



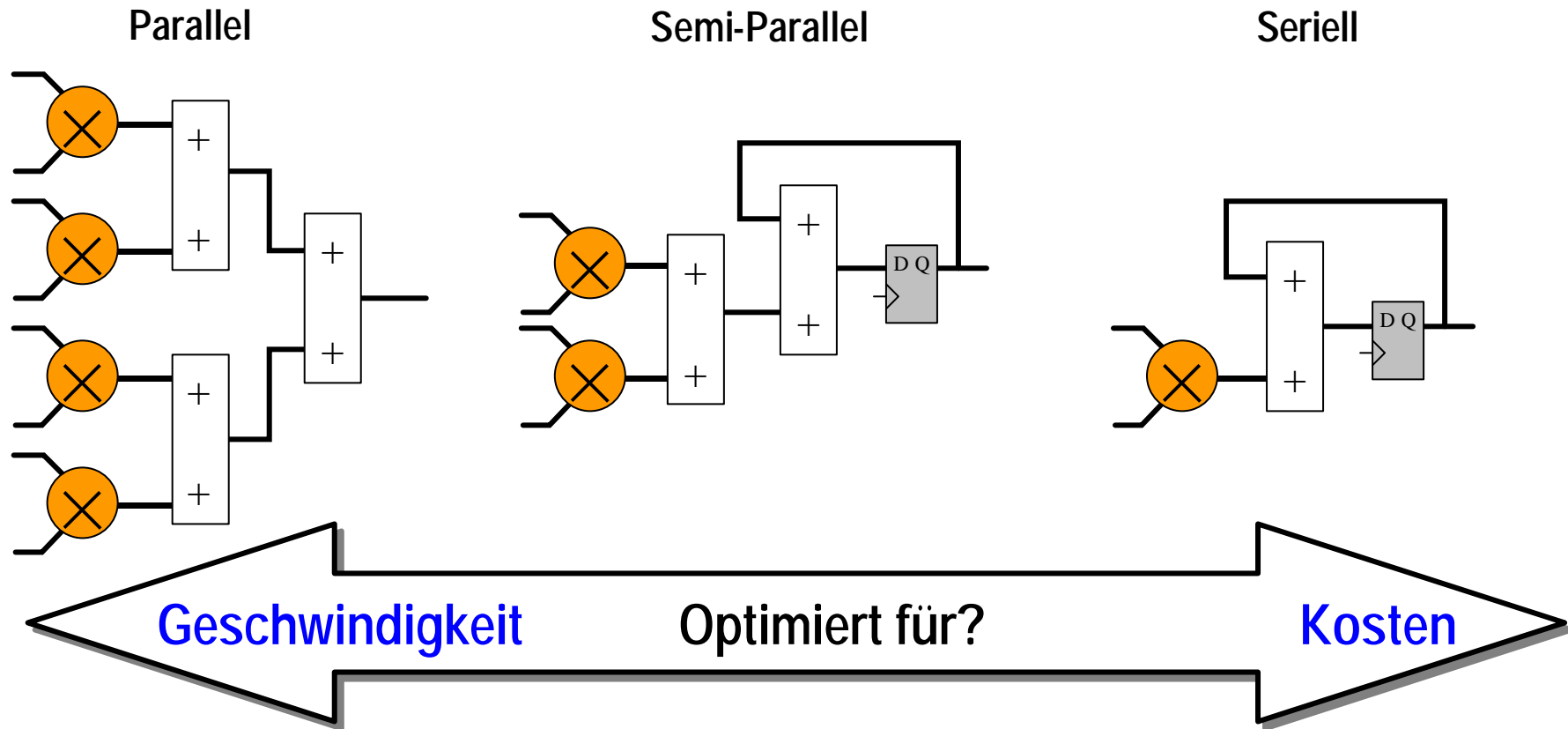
$$\frac{1 \text{ GHz}}{256 \text{ clock cycles}} = 4 \text{ MSPS}$$



$$\frac{256 \text{ MHz}}{1 \text{ clock cycle}} = 256 \text{ MSPS}$$



Flexible Architektur an den Algorithmus angepasst

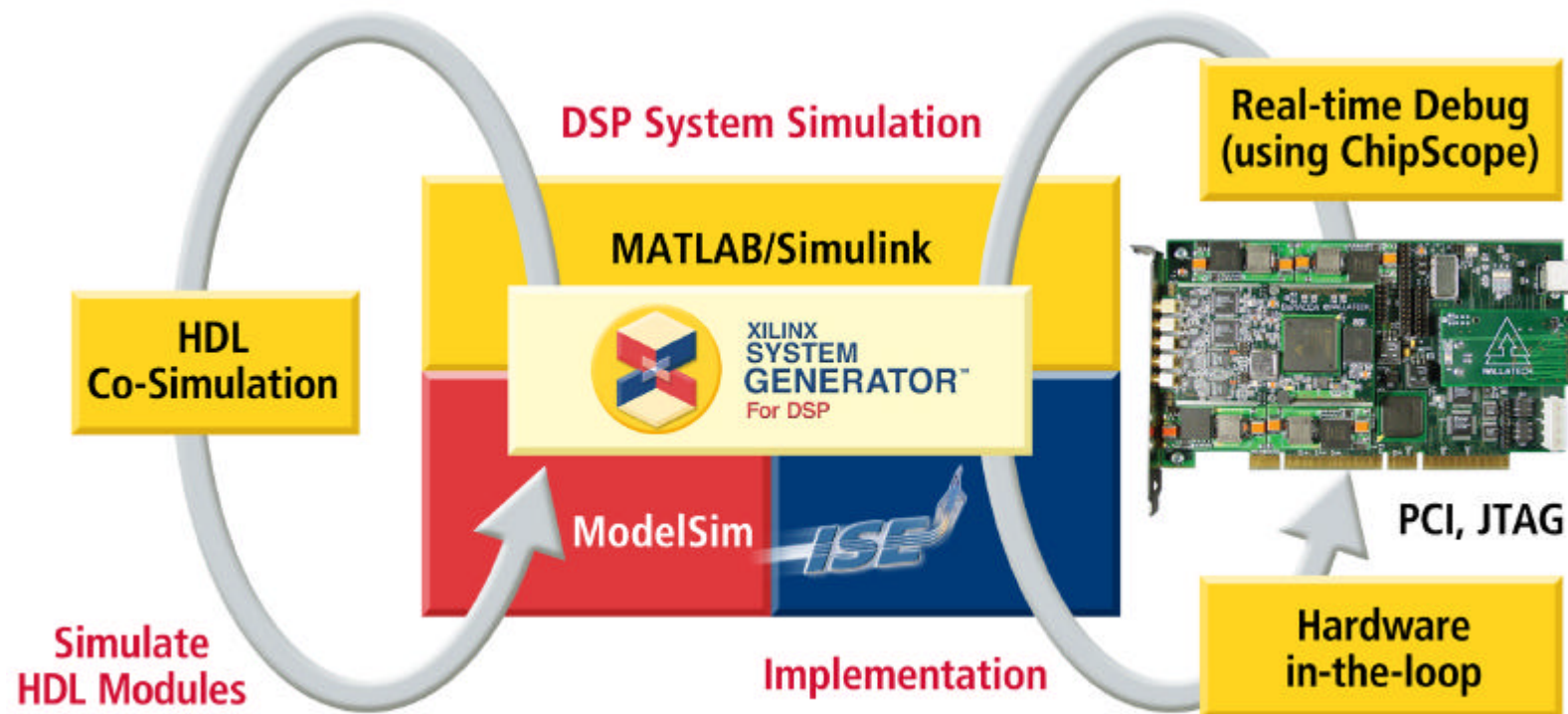


FPGAs erlauben Area / Performance Kompromisse





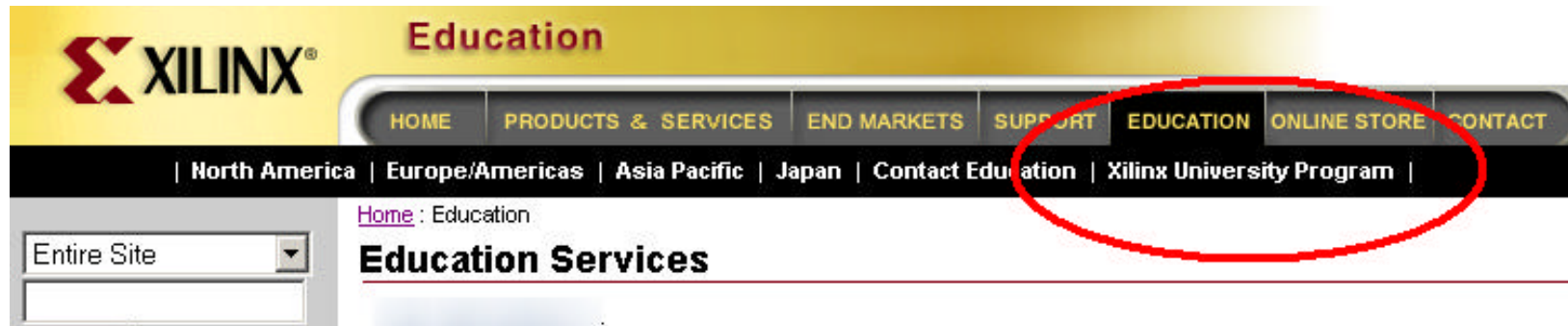
Xilinx System Generator für DSP



Vom Simulink zum FPGA Bitstream



Xilinx University Programm



- Donation Programm
 - Demoboards, Software, etc.
- Xilinx University Resource Center
 - Hands On Labs, Skripten für Lehrer und Schüler, ...
- Workshops
- Vergünstigte Konditionen
 - Demoboards, Entwicklungsplattformen, etc.





Spezielle Preise für Lehrzwecke

- ISE FND um 595 (250) USD
- Systemgenerator um 399 (359) USD
- Embedded Development Kit um 250 (200) USD
- Beliebig viele Workstations



Spartan-3 Starter Kit



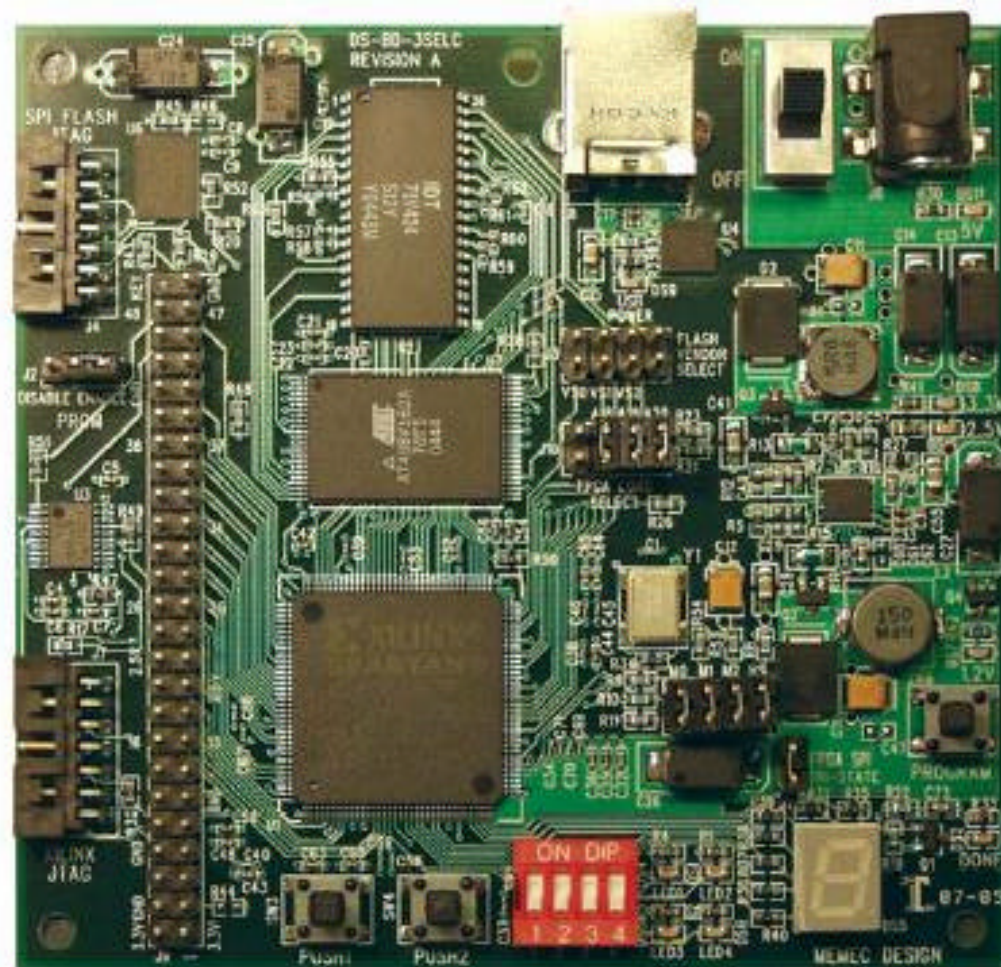
um 99 USD





Spartan-3E Low Cost

- 3S100E
- Ext. Flash
- SRAM
- Peripherie
 - USB, JTAG, ...
- 95 USD





Virtex-4 Low Cost

- 4VLX25
- LCD Display
- 10/100 Ethernet Phy
- 32Mx16 DDR SDRAM
- etc.
- 295 USD





Demoboards, Info, Preise

- Homepage

<http://legacy.memec.com/cgi-bin/devkits/international.cgi>

- Reference Design Center

Webserver, Demobeispiele, Schematics, BOM, ...

<http://legacy.memec.com/solutions/reference/xilinx/>





Fragen



The Programmable Logic CompanySM